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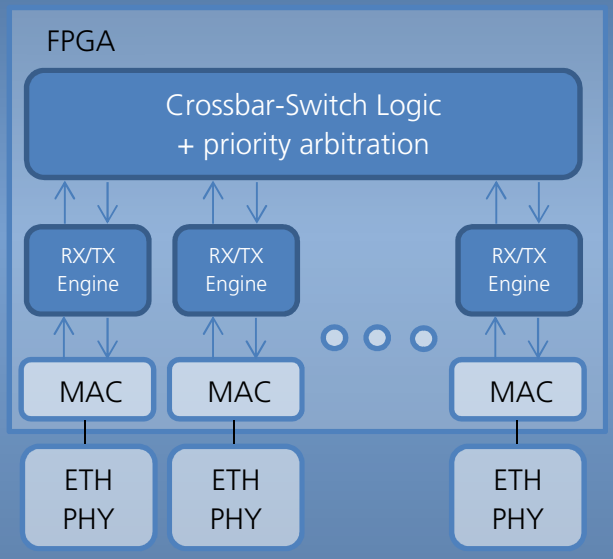
Ethernet Switch IP-core

Product Brief 1.1



Key Features

- 10/100/1000 Mbps
- Level2 Switching
- Interface to FPGA MAC
- Full Gigabit-Ethernet performance
- Crossbar-Switch logic for non-blocking parallel data transfers
- Configurable number of ports
- Optional diagnostic counters
- Custom packet handling, priorities etc. can be added

IP-core Description

The Ethernet Switch IP-core is a level 2 crossbar switch core which supports 10/100/1000 Mbit/s connections. Due to the level 2 switching, VLAN tags and other specialties are supported (transparent mode). The switch core can be used with MACs from Altera, Xilinx and Lattice.

The IP-core uses internal FPGA memory with a flexible pointer handling to maximize memory utilization. Buffer sizes are configurable to support jumbo frames. Packets are stored and inspected before forwarding, retaining low latency, to avoid transmission of broken frames.

The switch core can easily be adapted for custom packet filtering, priority switching and other custom requirements.

The IP-core has been deployed and proven in several industrial systems. Reference designs are available. Typical required design resources: depending on buffer sizes and MAC table size and diagnostic functions, approx. 1500 logic cells / port.

System Application

The Ethernet Switch IP-core is ideal for custom switching applications with special requirements considering packet filtering, monitoring, QoS and other higher level tasks. These tasks can be easily added to the existing level 2 switching behavior and priority mechanisms provided out of the box.

We can provide HDL source code or encrypted netlists as well as different license models, please contact af inventions for a quote or more information on flexible FPGA design solutions.

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